

WHAT IS CLAIMED IS:

1 1. A method of acquiring timing associated with an input data stream,
2 comprising:
3 detecting whether transitions of the input data stream fall into a predetermined
4 portion of a sample clock period of a sample clock utilized to sample
5 the input data stream; and
6 evaluating whether a phase-locked loop (PLL) has acquired the timing of the
7 input data stream according to occurrence of transitions of the input
8 data stream in the predetermined portion of the sample clock period.

1 2. The method as recited in claim 1 wherein the evaluating further
2 comprises determining over a plurality of time periods, each of the time periods
3 including an increasing number of evaluation intervals, whether the PLL is locked to
4 the timing of the input data stream according to a number of evaluation intervals
5 having one or more transitions in the predetermined portion of the sample clock
6 period.

1 3. The method as recited in claim 1, wherein the sample clock is a clock
2 recovered from the input data stream.

1 4. The method as recited in claim 1, wherein the evaluating includes
2 counting a number of evaluation intervals that have at least one transition in the
3 predetermined portion of the clock period, generating a count indicative thereof and
4 determining if lock is achieved according to the count.

1 5. The method as recited in claim 4 wherein the evaluation intervals are at
2 least as long as a minimum period of frequency offset.

1 6. The method as recited in claim 4, further comprising comparing the
2 count to a threshold count to determine if lock is achieved.

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1 16. An integrated circuit comprising:
 2 means for detecting whether transitions of an input data stream fall into a
 3 predetermined portion of a clock period of a clock utilized to sample
 4 the input data stream; and
 5 means for evaluating whether a phase-locked loop (PLL) has recovered a
 6 timing associated with the input data stream according to occurrence of
 7 transitions in the predetermined portion of the clock.

1 17. The integrated circuit as recited in claim 16 means for evaluating
 2 includes means for counting a number of evaluation intervals that have one or more
 3 transitions that fall into the predetermined portion of the clock period, generating a
 4 count thereof and determining if lock is achieved according to the count.

1 18. The integrated circuit as recited in claim 16, further comprising means
 2 for changing an output frequency of a variable oscillator circuit if it is determined that
 3 lock is not achieved.

1 19. A method of acquiring a clock embedded in an input data stream,
 2 comprising varying an output of a variable oscillator until transitions of the input data
 3 stream occurring in a predefined phase zone of a sample clock sampling the input data
 4 stream occur below an acceptable rate.

1 20. The method as recited in claim 19 wherein the acceptable rate is
 2 determined according to a number of evaluation intervals having one or more
 3 transitions occurring in the predefined phase zone.

1 21. The method as recited in claim 19 wherein the output of the variable
 2 oscillator is varied by varying an impedance of the variable oscillator.

1 22. The method as recited in claim 19 wherein varying the output of the
 2 variable oscillator comprises varying at least one of a control voltage and a control
 3 current supplied to the variable oscillator.

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34. The integrated circuit as recited in claim 23 wherein the oscillator circuit is ring oscillator.

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